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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,952	01/30/2004	Masayoshi Kodama	61282-058	2496

20277 7590 10/03/2007

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
10/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,952	KODAMA ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,3,4,13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawai (patent No. 6,240,358).

Kawai taught the invention as claimed including a data processing ("DP") system comprising:

a) Storing an internal information of CPU in a task stack of a task to be interrupted as a first area in accordance with the generation of an interruption (e.g., see fig.7 and col. 8, lines 5-59);

b) Storing a value of a stack pointer after storing the internal information in a prescribed first position of a interrupt processing stack (e.g., see figs.7,8);

c) Setting the stack pointer to a prescribed second position in the interrupt processing stack (e.g., see fig. 7, and col. 2, lines 1-34); and starting an interrupt process (e.g., see fig.8), wherein the prescribed second position of the interrupt processing stack corresponds to a prescribed position in the first area in the task stack of a specific task (e.g., see fig. 8, and col. 9, lines 7-20).

3. As per claim 3, Kawai taught the prescribed first position of the interrupt processing stack is the top address of the interrupt processing stack (e.g., see fig. 7 and col. 8,lines 36-59).

4. As per claim 4, Kawai taught the prescribed second position of the interrupt processing stack is immediately after the prescribed first position of the interrupt processing stack (e.g., see figs. 8,10 and col. 9, lines 7-52)[when interrupt arises while task C is being processed the prescribed second position is immediately after the prescribed second position].

5. As per claim 13, Kawai taught a stack controller of a multitask system in which information in a CPU is stored in the task stack (e.g. see col. 3, lines 38-67) of a task to be interrupted in accordance with the generation of an interrupt to have a first area (e.g., see col. 8, lines 5-23), the value of a stack after the storage in the first area is stored in a prescribed first position of an interrupt processing stack and the stack pointer is set to a prescribed second position of the interrupt processing stack to start an interrupt process (e.g., see fig. 7 and col. 8, lines 23-47), wherein an control mechanism is provided by which the top address of the interrupt processing stack is allowed to correspond to a prescribed position in the first area in the task stack of a specified task (e.g., see figs. 7,8, and col. 8,lines 5-67 and col. 9, lines 7-42).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2,5-8,12,14,15-18,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai as applied to claim 1,3,4,13, above, and further in view of Ebrahim (patent No. 5,893,121).

8. As per claims 2,5,14,15 Ebrahim taught the first area includes a second area for storing task control information necessary for a return control from an interrupt process (return address PC, previous frame PC) and a third area disposed immediately after the second area to store internal information of the CPU (current ev, Stack pointer)except the task control information, and the prescribed position area in the task stack of the specific task corresponds to the top address of the third address of the third area in the first (e.g., see col. 12, lines 8-50 and col. 13, lines 7-59) and Kawai taught and area that is obtained by correcting the top address of the third area in the first area by a prescribed difference value (e.g., see col. 9, lines 7-52).

9. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Kawai and Ebrahim. Both references were directed toward the problems of controlling tasks using stacks in a DP system. One of ordinary skill would have been motivated to incorporate the Ebrahim teaching of including controlling information in the stack where this at least would have allowed the combined system more completely provide data necessary for a system to recover from an interrupt.

10. As per claims 6,16 Kawai taught the address different is given to designate an area for storing internal information of the CPU used in the specific task ([500bytes in task C region in fig. 5). As per claims 7,17 Kawai taught the difference is previously given as a constant (e.g., see col. 3, lines 2-28). As per claim 8,18 Kawai taught the difference is set by executing the specific task (e.g., see col. 3, lines 2-28) The size is set to a maximum when there is only one task but when there are multiple tasks the task regions are set to the size necessary to process the individual tasks].

11. As per claim 12, the Kawai did not expressly detail the claimed location of storing the task data. However since the Kawai stored the claimed task data and comprised the regions for storing data then the operation and structure of the system is the same.

12. As per claim 19, Kawai did not expressly detail a compiler for implementing the processing system or by forming the address difference value. However Kawai taught the maximum is set for the size of task area or the difference in addresses where the different tasks are stored. Therefore since the Kawai system was a programmed system then one of ordinary skill would have been motivated to implement the forming of the difference by a compiler since the difference is constant.

13. Claims 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai and Ebrahim as applied to claims 1,2 above, and further in view of Matsuzaki (patent No. 5,966,514).

14. As per claim 9, Matsuzaki taught the task control information includes at least one program counter and a program status word (e.g., see fig. 19B)

15. It would have been obvious to one of ordinary skill in the DP system to combine the teachings of Kawai and Matsuzaki. Both references were directed toward the problems of controlling tasks using stacks in a DP system. One of ordinary skill would have been motivated to incorporate the Matzuzaki teaching of including program status word with and return program counter in the stack during interrupt processing at least to allow the combined system more completely provide data necessary for a system to recover from an interrupt.

16. Claims 10,11,are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai.

17. As per claim 10,Kawai taught a system that interrupted tasks in a DP system and an interrupt cyclically started (e.g., see col. 7, lines 51-67). Clearly when a task was idle it would have been of the lowest priority. Therefore it would have been obvious to one of ordinary skill that idling task would have been task that would have preferentially been interrupted in the Kawai system.

18. As per claim 11, Kawai taught the computer powered by a battery e.g., see col. 5, lines 39-67) therefore one of ordinary skill would have been motivated to provide the specific task for controlling shift and return to a low power consumption mode.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kudo (patent No. 6,560,692) disclosed a system with stack storing data and stack pointers (e.g., see abstract and fig. 4).

Toy (patent No. 4,386,402) disclosed a computer with dual vat buffers for accessing common memory shared by a cache and a processor interrupt stack (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER